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Quantum error correction beyond the surface code

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WERQSHOP 2025

Joint work with Qian Xu*, Chris Pattison, Nithin Raveendran, Dolev Bluvstein, Jonathan Wurtz, Bane Vasic, Mikhail Lukin, Liang Jiang, Hengyun (Harry) Zhou. **Nat. Phys.** 20, 1084-1090

Challenge of Large-Scale Quantum Computation

Quantum error correction will
bridge this gap!

Physical error
rates today

What large-scale quantum
algorithms require

10^{-1}

10^{-2}

10^{-3}

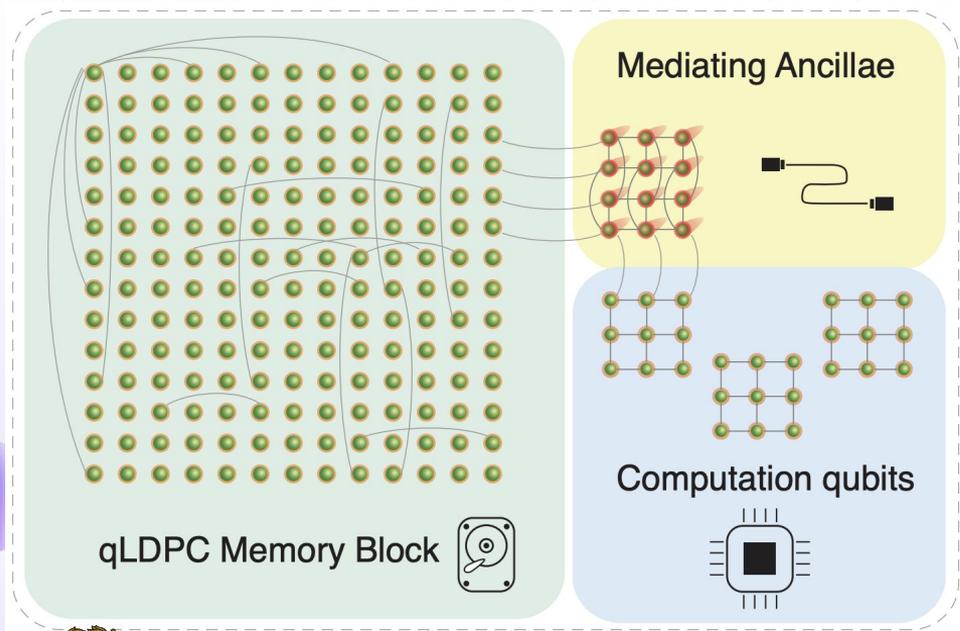
10^{-15}

Error rate of
encoded qubit

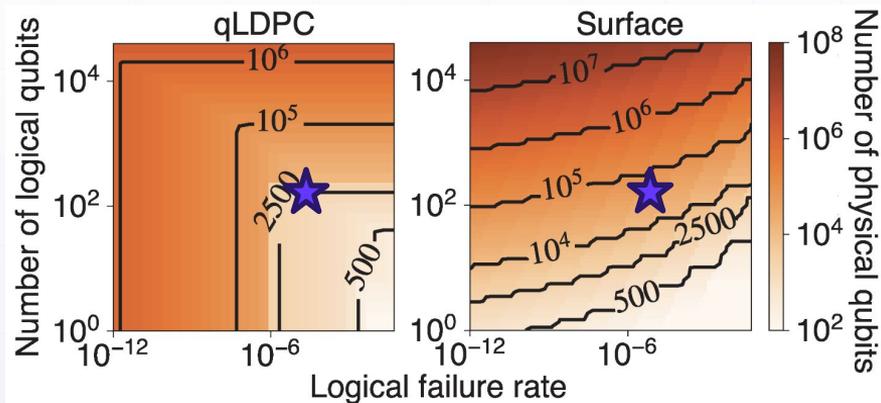


This Work: Bridging the Gap with qLDPC Codes

Implementation blueprint for memory & logical gates on a neutral atom quantum computer



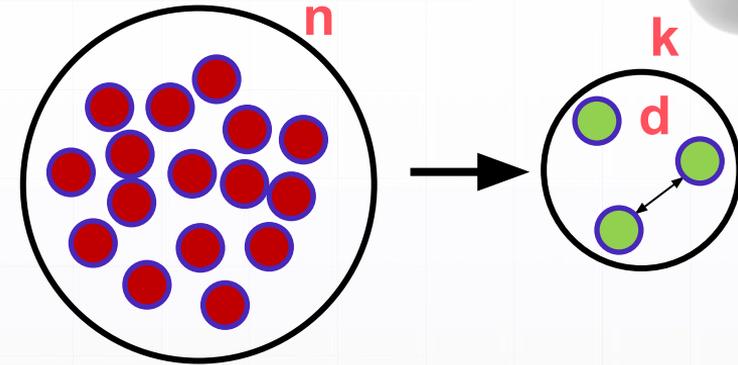
- Order of magnitude fewer physical qubits required, when replacing surface code with qLDPC code



Beyond the surface code?

- Good codes: $k = O(n), d = O(n)$
- Surface code: $k = O(1), d = O(\sqrt{n})$
- Best 2D-local codes: $kd^2 \leq O(n)$ (saturated by surface code)
- For improved properties: need non-locality!
- ... while preserving ldpc-ness (constant check weight + qubit degree)

The main message is that magic state distillation is *not* the dominant cost in a surface-code-based quantum computer. Rather, the large overhead of surface codes is due to their low encoding rate, which implies that a large number of qubits is required to simply store all data qubits of the computation. Litinski, Quantum (2019)



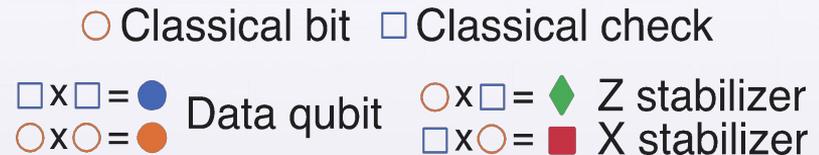
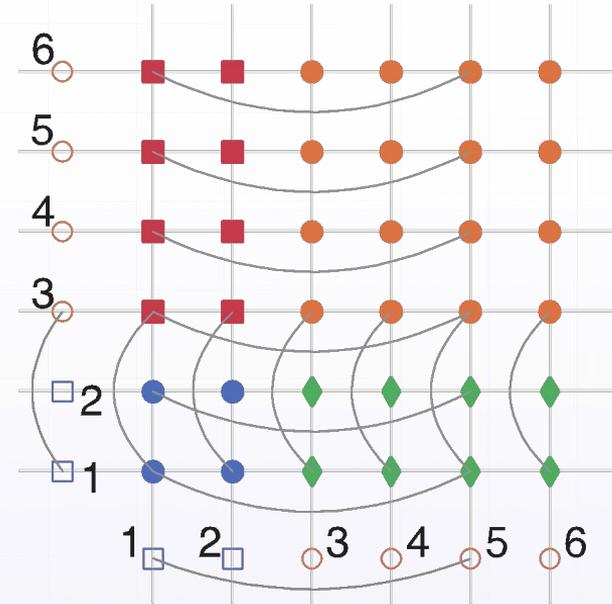
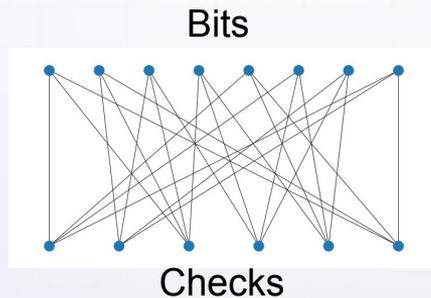
[[n, k, d]] quantum code:

- n : number of physical qubits
- k : number of logical qubits
- d : code distance (error-correcting power)
- $R=k/n$: code rate



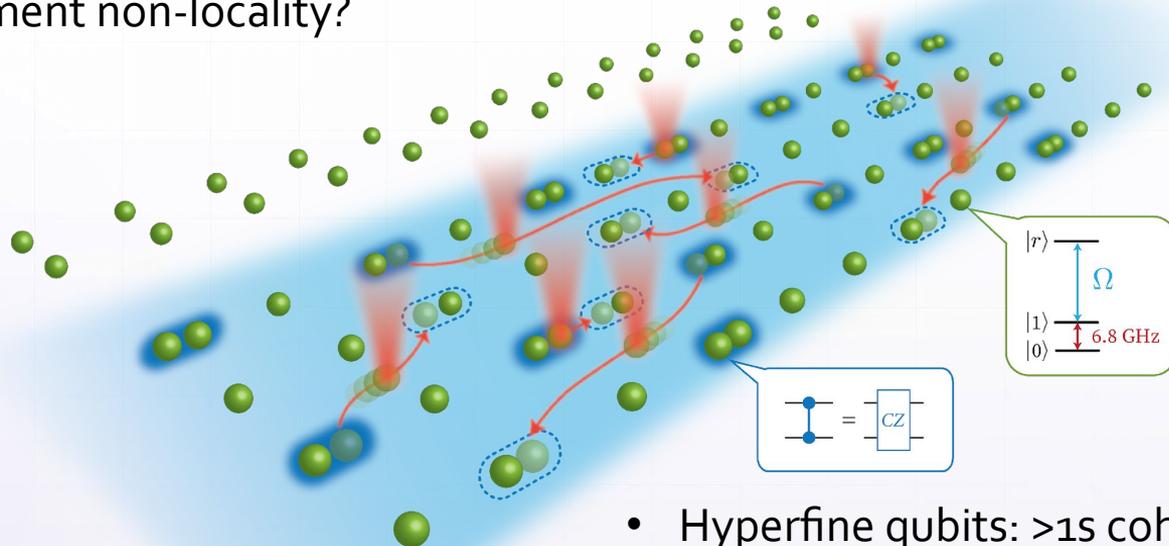
Product Structure of Some qLDPC Codes

- Hypergraph product code (HGP):
 - Construct quantum code by taking product between two classical codes
 - Example: surface code = HGP of two repetition codes
- Taking HGP of two classical codes with $[n, k = \Theta(n), d = \Theta(n)]$, we obtain a quantum code $[[n, k = \Theta(n), d = \Theta(\sqrt{n})]]$
 - In this work: random (3,4)-biregular graphs



Dynamically Reconfigurable Architecture with Neutral Atoms

How to implement non-locality?

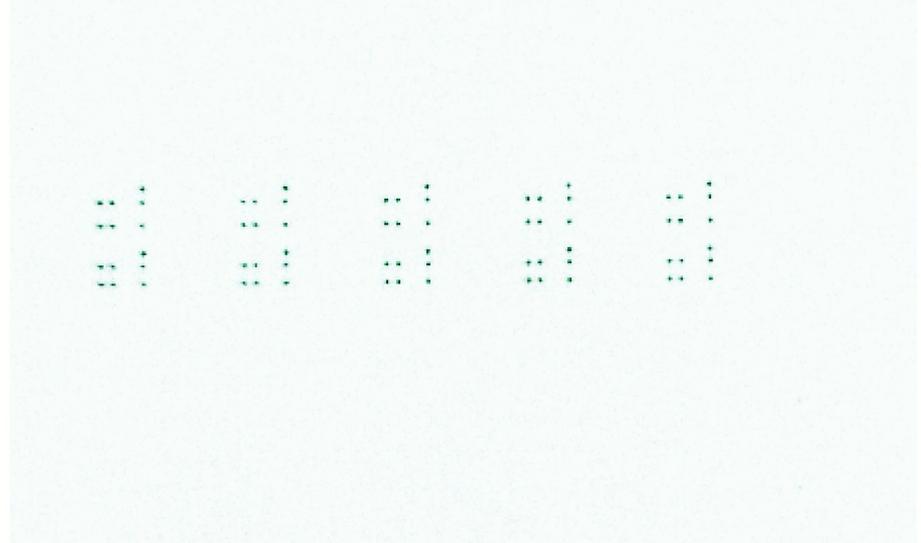
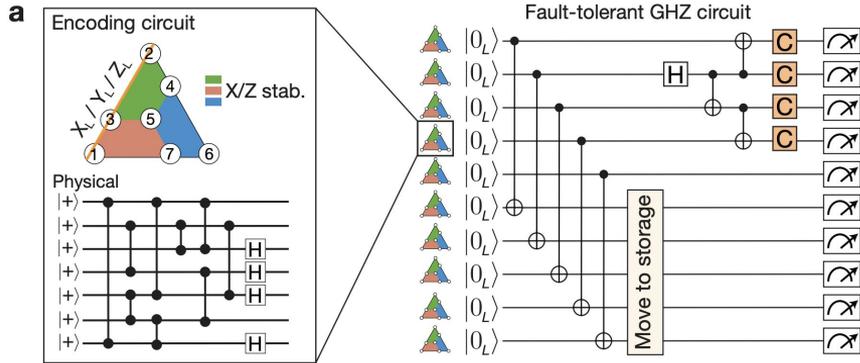


- Hyperfine qubits: $>1s$ coherence, $\sim 99.98\%$ global 1Q, $\sim 99.9\%$ local 1Q
- Rydberg-mediated two-qubit gates $\sim 99.5\%$



Unique opportunities for error correction with reconfigurable atom arrays

Example: GHZ state with logical qubits

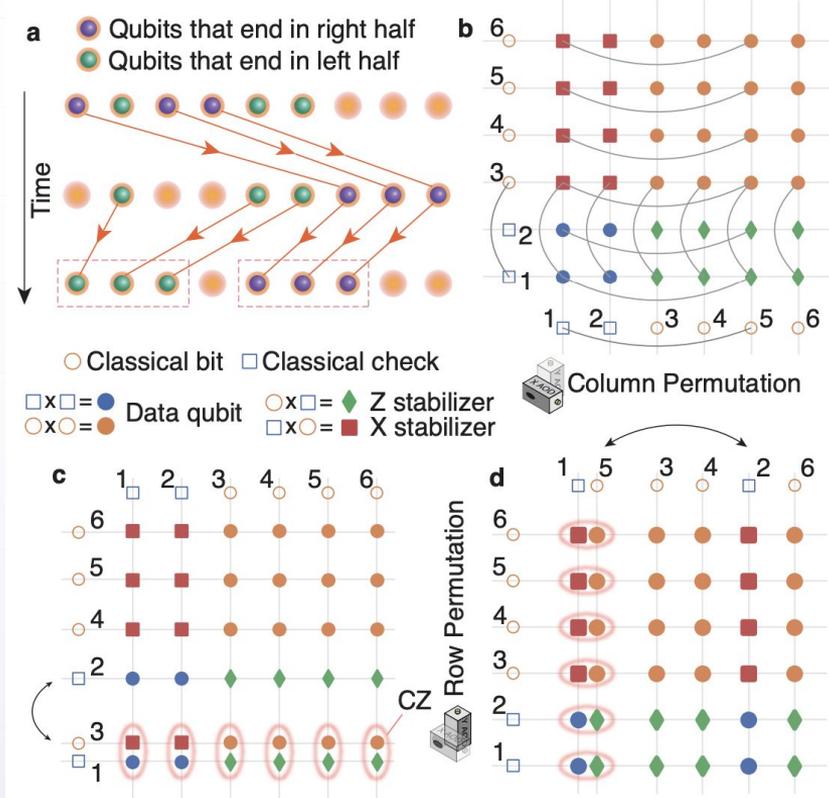


Enabling feature: efficient parallel classical control!



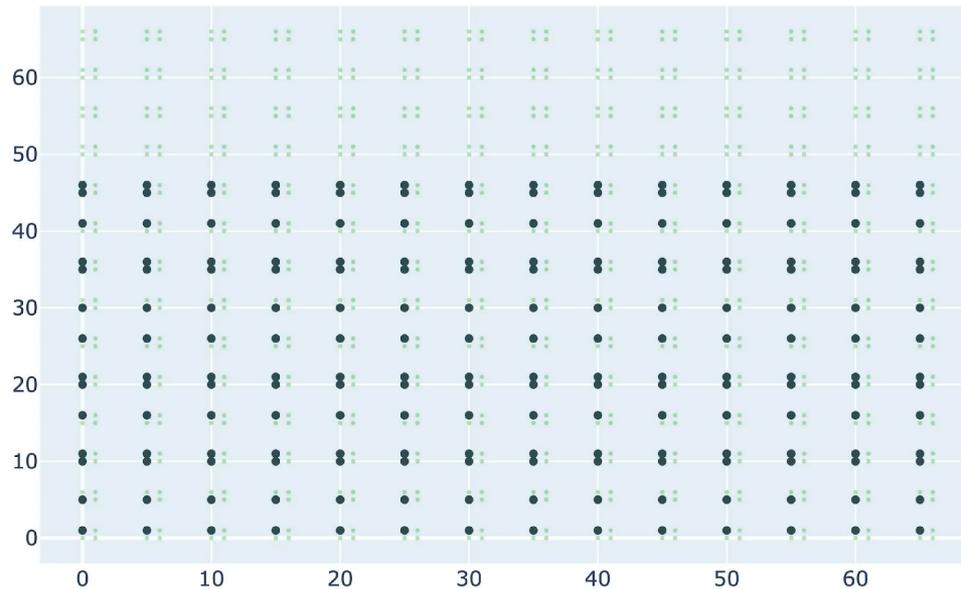
Implementing the Product Structure of HGP codes

- Key insight: product structure of codes matches well with product structure of optical tools (AODs)
- For each check:
 - Permute columns, do CZ gates
 - Permute rows, do CZ gates
- Efficient 1D rearrangement:
 - L qubits in a line
 - At each step:
 - Move to the right half qubits that in the end configuration appear in the right half
 - Repeat within each new half
 - #moves = $O(\log L)$



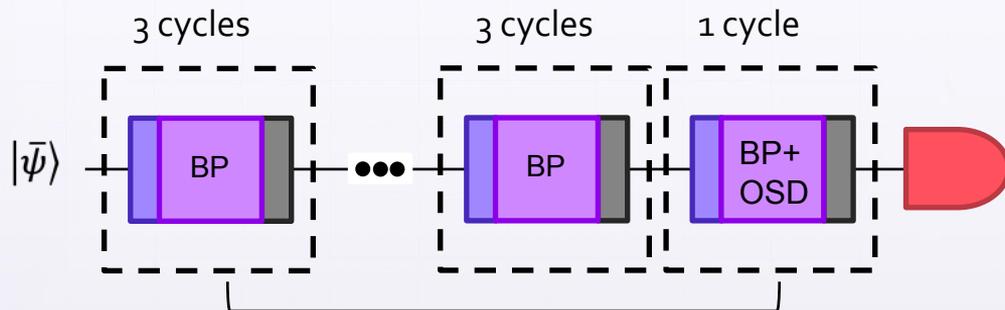
Full Layout for Hypergraph Product Code

- Very generic compilation and with current optical tools
- Movie generated using experimental software and commands!

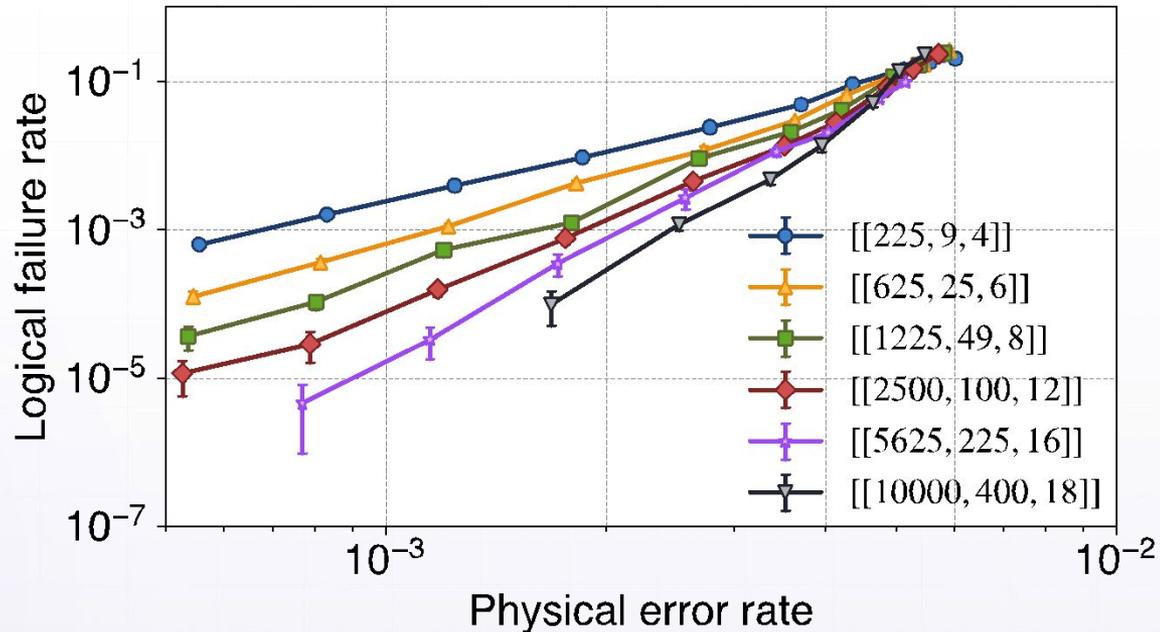


Circuit-Level Performance Evaluation

- Memory simulations: keep logical qubit alive for a long time
- HGP codes satisfy linear syndrome confinement:
 - “Qubits errors cannot grow without triggering more measurement syndromes”
- Confinement + bounded check weight:
 - Single-shot decoding
 - Single-ancilla syndrome extraction is fault-tolerant
 - We prove the existence of a threshold under these considerations!
- BP + BP-OSD decoding on circuit-level detector error model
 - Joint decoding of multiple rounds to improve performance



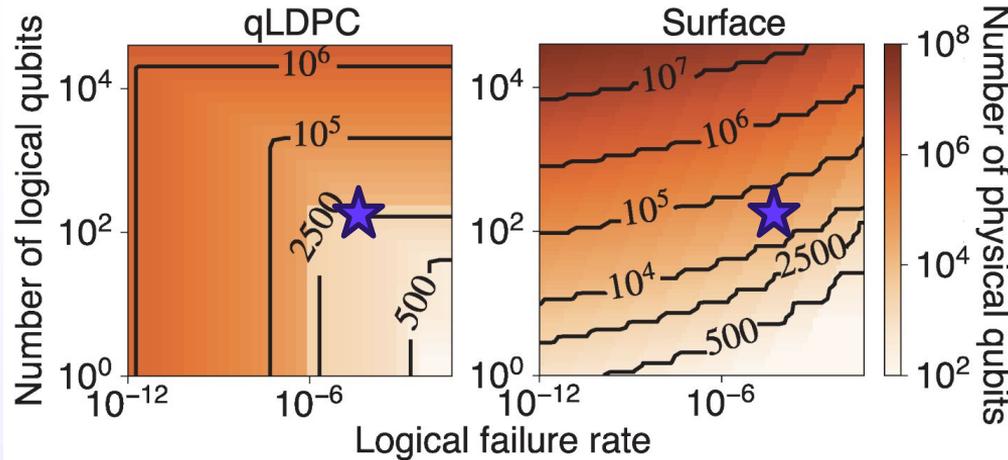
Competitive Memory Circuit-Level Performance



- Error threshold $\sim 0.6\%$ under circuit-level depolarizing noise without idling errors
- Long neutral atom coherence times \rightarrow adding in realistic idling errors (that scale with code size) produces minimal changes



Competitive Circuit-Level Performance



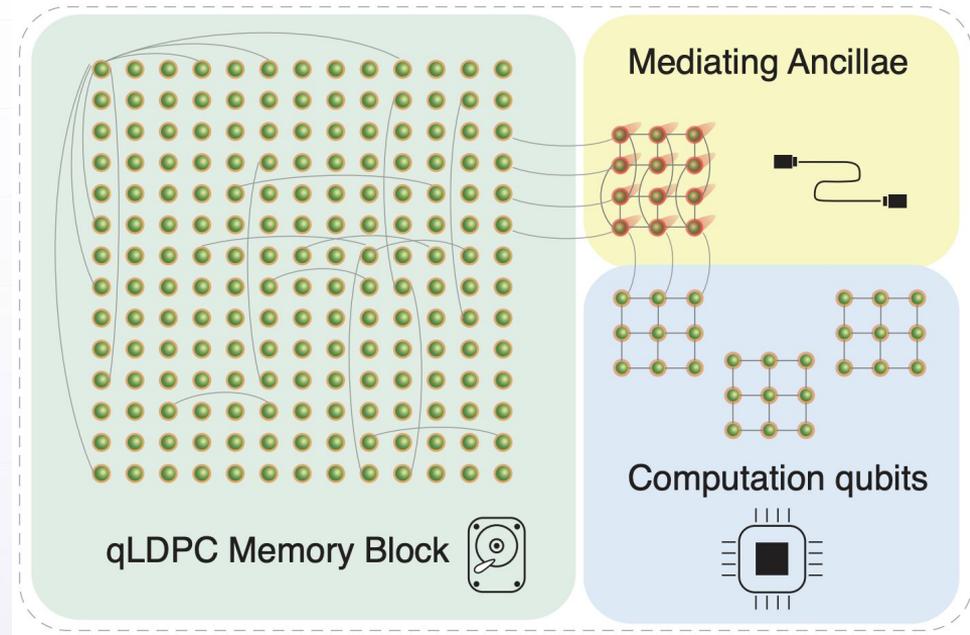
- qLDPC codes start out-performing surface codes at **several hundred physical qubits** and 0.1% error rates
- **Orders of magnitude** savings!
- <100k qubits enough for 1000 logical qubit computation!

Logical qubits	25	80	180	400
Logical failure rate	10^{-3}	10^{-4}	2×10^{-5}	6×10^{-6}
HGP code physical qubits (improvement over surface code)	1235 (1×)	4606 (2.8×)	10760 (4.0×)	19600 (6.9×)
LP code physical qubits (improvement over surface code)	851 (1.4×)	1367 (9.4×)	2670 (16.2×)	



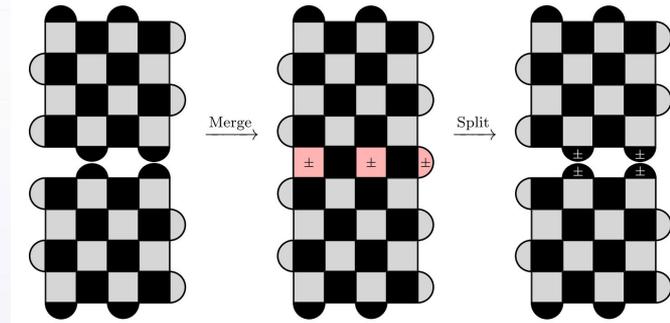
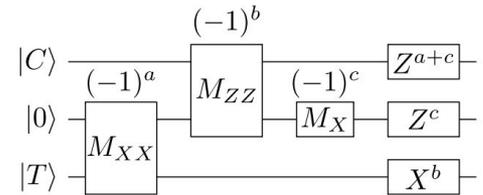
Computation with Logical Qubits

- qLDPC: memory
- Topological codes: processor
- Small enough number of computational qubits in parallel:
 - Can maintain constant overhead
- Our contribution:
 - Qubit efficient teleportation $\text{qldpc} \leftrightarrow \text{surface}$
 - First numerical simulations of computation with qLDPC codes



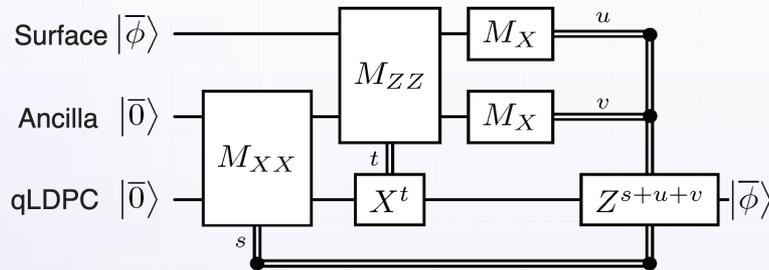
Lattice surgery

- Measurement-based gates: universal
 - Need: single and joint (logical) Clifford measurements
- Trick – for codes of similar boundary:
 - Merge codes
 - Logical measurement becomes stabilizer of new code
 - Measure stabilizer fault-tolerantly
 - Split codes
- Teleportation: also through measurement
 - Boundary of qLDPC and surface code can be very different
 - How to merge to perform joint measurement?

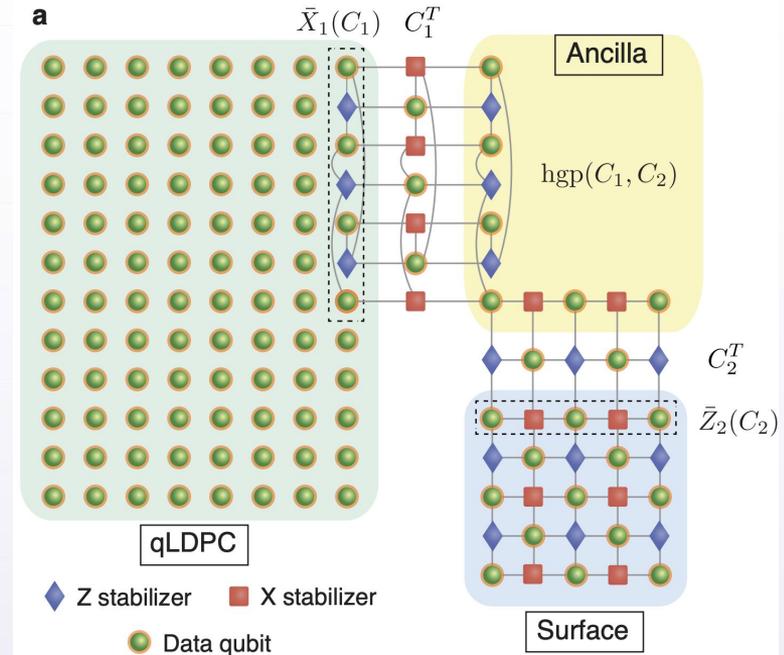


Teleportation through Lattice Surgery

- Mediate teleportation with ancilla block. Treat logicals as classical codes
- Ancilla block: HGP again!
- Logicals of same type:
 - Normal lattice surgery

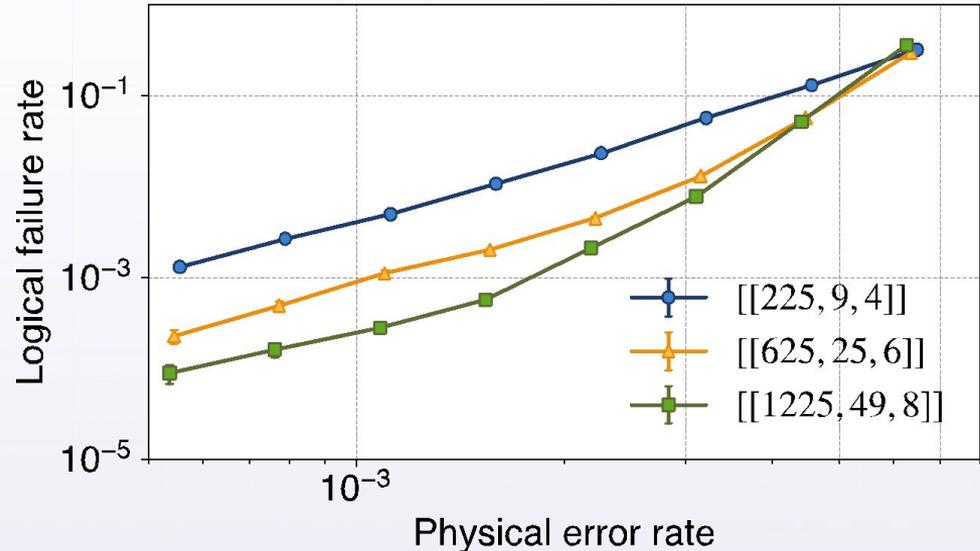
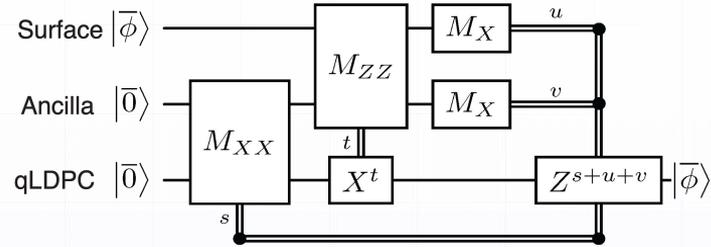


N.B. We prove this procedure is fault-tolerant



Lattice Surgery Performance

- Teleport logical qubits into surface code for computation
- Circuit-level simulations of teleportation process
- **Competitive threshold and error rates maintained!**

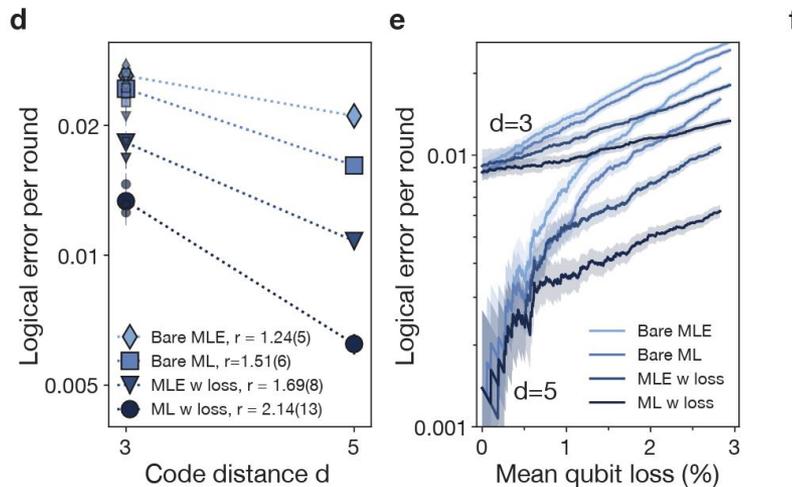


Outlook

Exploring LDPC challenges and opportunities on near-term hardware

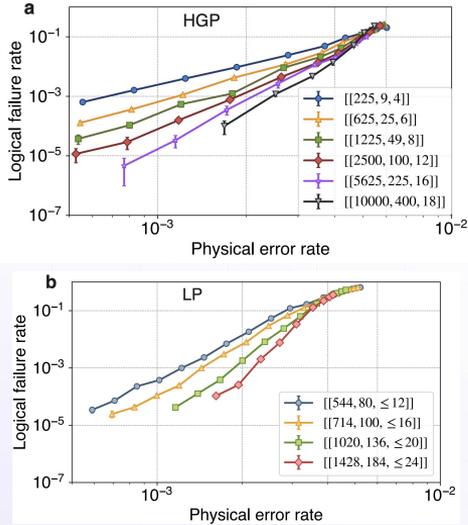
- Space-time trade-offs
- Improving qLDPC computation
- How to incorporate QEM into these
 - QEM largely unexplored in neutral atom
 - Some ideas: QEC naturally projects noise needed?), extrapolation based on posts

2x below surface-code threshold

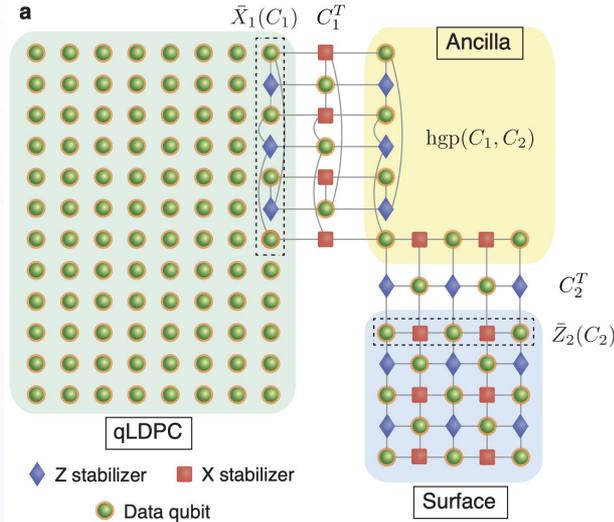


Summary

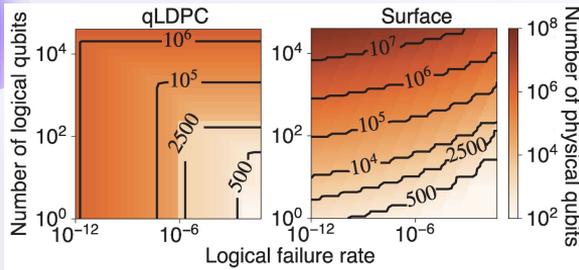
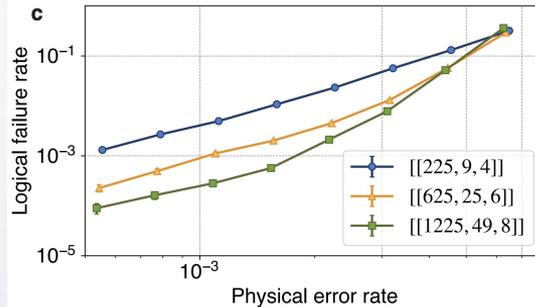
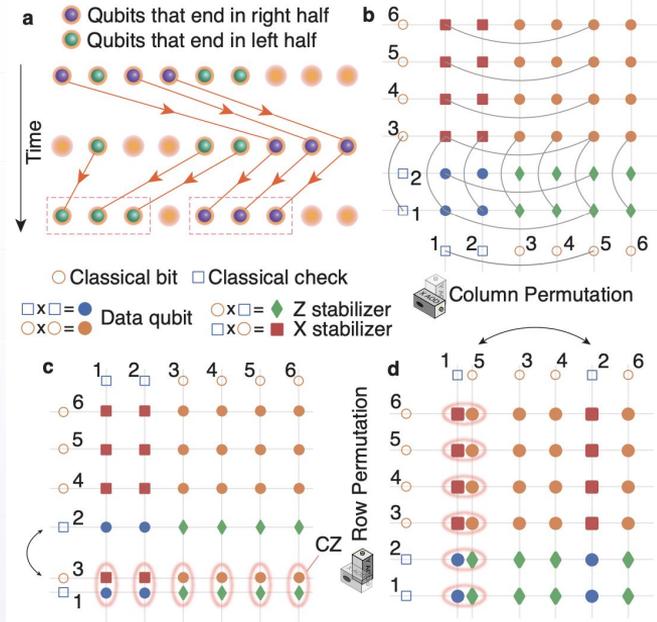
Memory



Gates



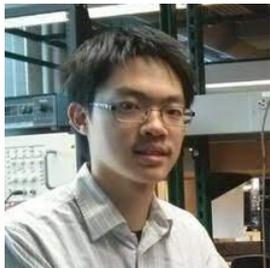
Practical implementation



Collaborators



Qian Xu
(U.Chicago)



Harry Zhou
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Chris Pattison
(Caltech)



Liang Jiang
(U.Chicago)



Mikhail Lukin
(Harvard)



Dolev
Bluvstein
(Harvard)



Nithin
Raveendran
(Arizona)



Jonathan Wurtz
(QuEra)



Bane Vasic
(Arizona)

Thanks also to other members of Harvard atom array team.



