WERQSHOP 2025

Error Mitigation for Logical Qubits

Probabilistic Error Cancellation

Part 1: Error-Detected Qubits
Part 2: Error-Corrected Qubits

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- **Joint work with**: Steve Girvin (Yale), Rob Schoelkopf (Yale), Aleksander Kubica (Yale), and their group members.
- **Disclosure**: YD is a consultant to Quantum Circuits, Inc.

Simple Error Mitigation Strategy

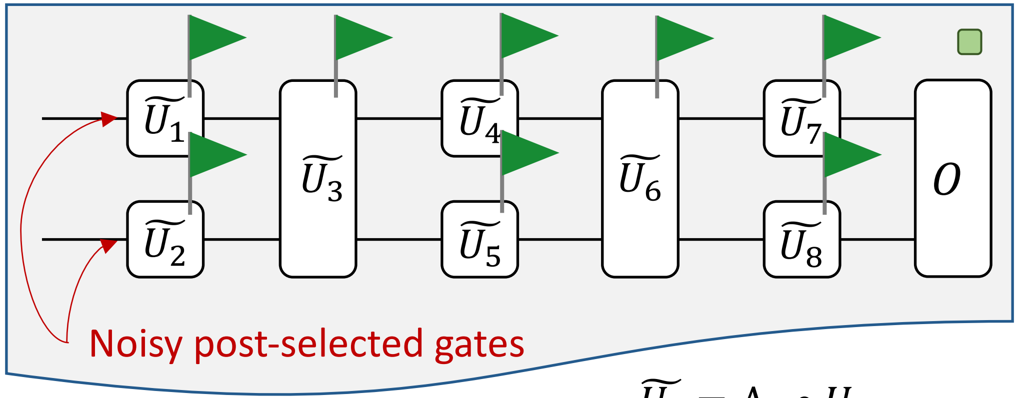
1. **Detect** dominant error (e.g., leakage): ϵ_1
2. Then **mitigate** residual error: ϵ_2

Error Detection (ED):
Discard erroneous circuit samples

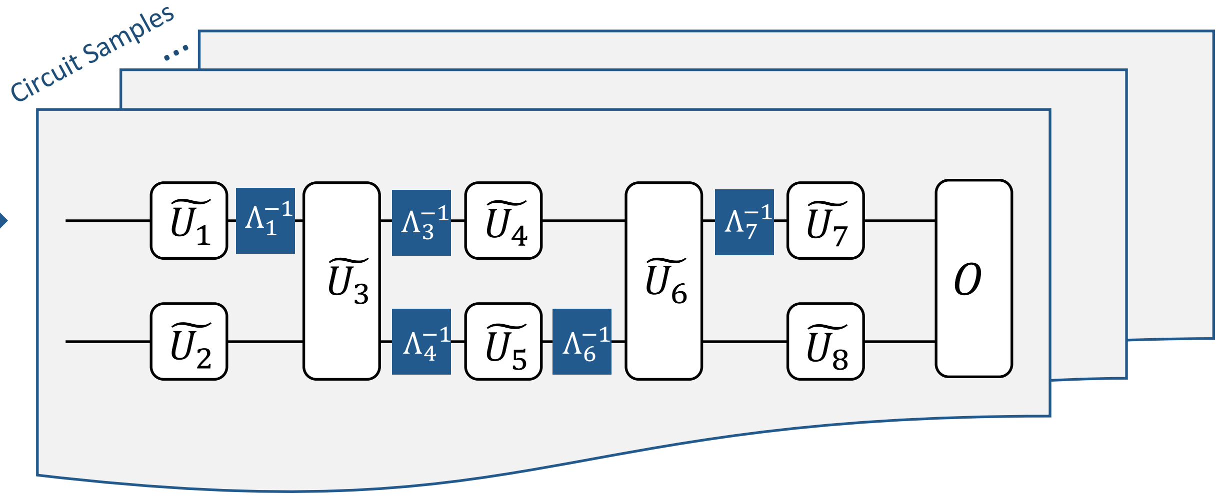
- Post-selected circuit fault rate: $O(M\epsilon_2)$
- Acceptance probability: $p_{\text{accept}} = e^{-M\epsilon_1}$
- **Sampling overhead**: $C_{ED} = e^{M\epsilon_1}$

Probabilistic Error Cancellation (PEC) [1,2]:
Average over noisy circuit samples

- Unbiased estimator of $\langle O \rangle$: $|\mathrm{Tr}[O\rho] - \mathrm{Tr}[O\rho_{\text{PEC}}]| \to 0$
- **Sampling overhead**: $C_{\text{PEC}} = \prod_1^M \left(\frac{1+\epsilon_2}{1-\epsilon_2}\right)^2 \approx e^{4M\epsilon_2}$



$\widetilde{U}_c = \Lambda_c \circ U_c$



[1] Temme et al. PRL (2017), [2] S. Endo et al. (2018)

Numerical Simulation

Code-capacity error model of code distance d=2 with (idealized) large noise hierarchy

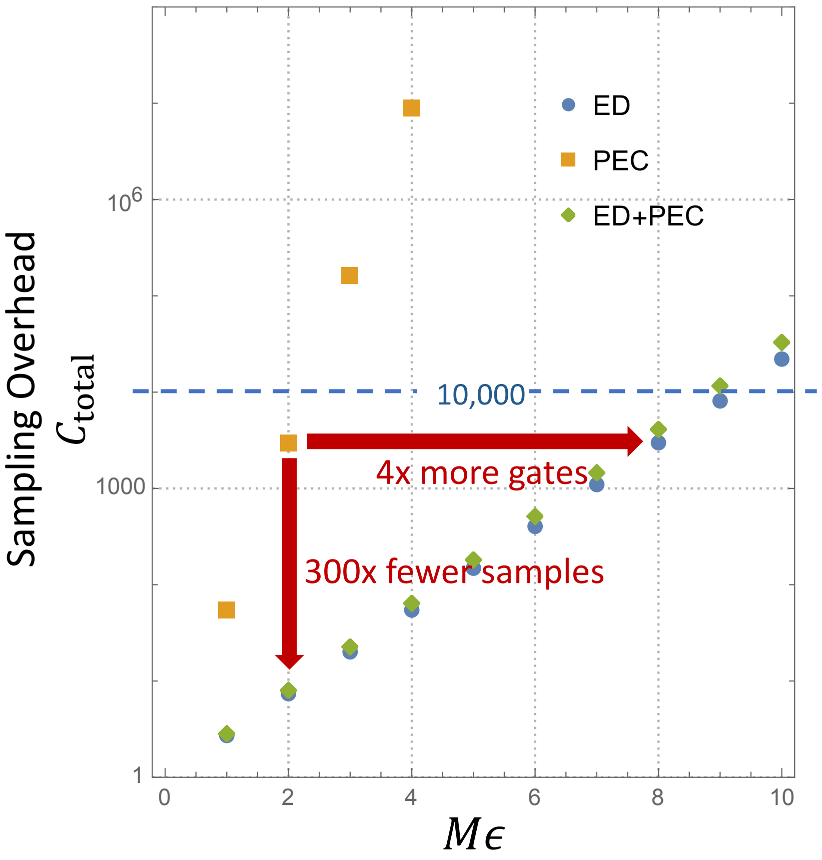
1. **Detect** dominant error (e.g., leakage): $\epsilon_1 = \epsilon = 10^{-3}$
2. Then **mitigate** residual error: $\epsilon_2 = \epsilon^2 = 10^{-6}$

Sampling overhead scaling:

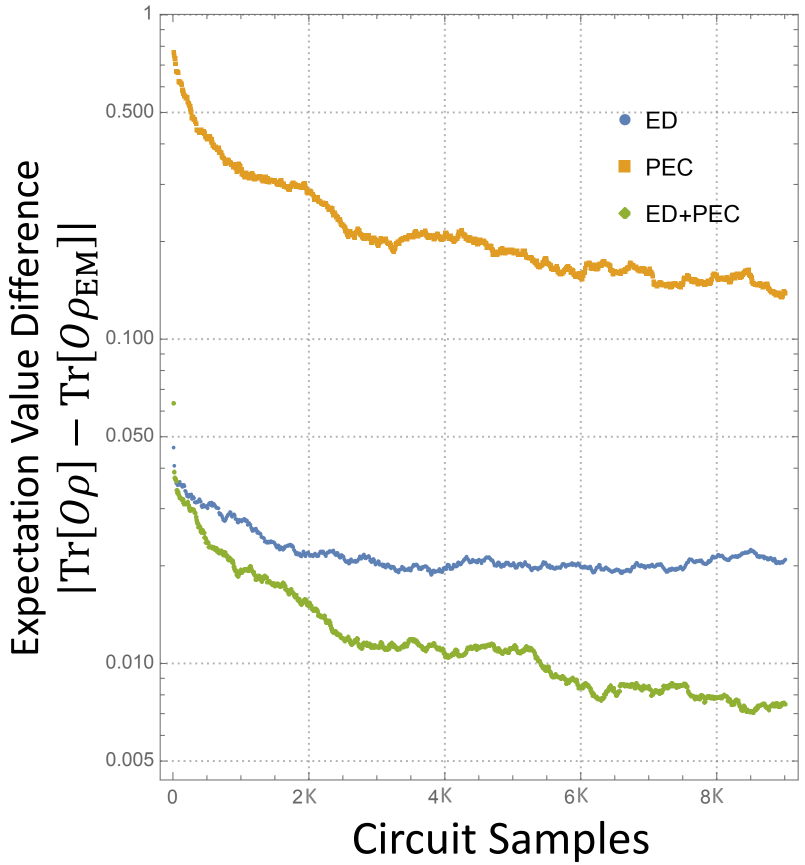
ED alone: $\exp(M\epsilon)$

PEC alone: $\exp(4M\epsilon)$

ED+PEC: $\exp(M\epsilon + 4M\epsilon^2)$



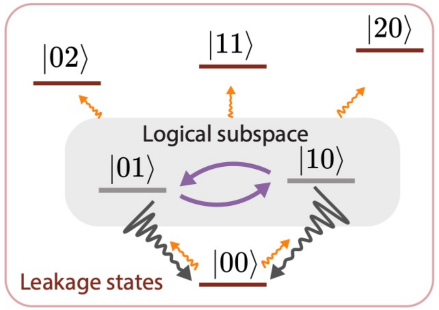
Focusing on circuit size M, where $M\epsilon \approx 1$

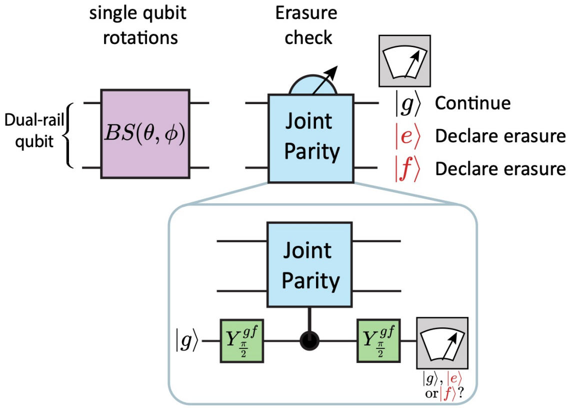


Error Detected Qubits

Logical subspace and **leakage subspace**: detecting leakage.

DUAL-RAIL QUBIT
(detect any single photon loss)

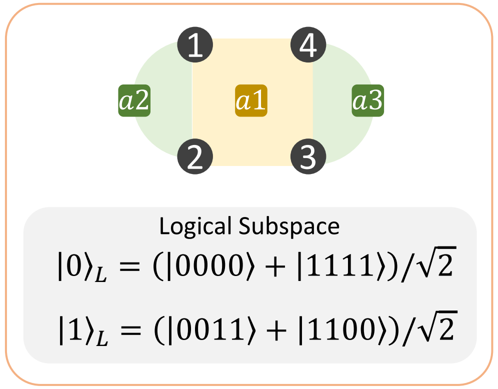


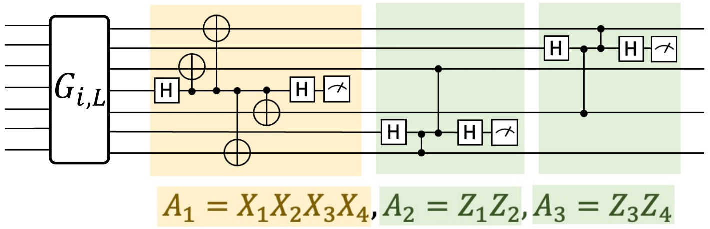


DR simulation*
(erasure check)

No Error	97.1%
Detectable Error	2.8%
Undetectable Error	0.1%

FOUR-QUBIT CODE
(detect any single X/Z error)





[[4,1,2]] simulation*
$(\varepsilon_{2Q} = 5\times10^{-3})$

No Error	80.4%
Detectable Error	11.5%
Undetectable Error	8.1%

K. Chou et al. Nature Physics 2023. J. Teoh et al. PNAS 2023.
Lu, Maiti, et al. Nat Comm, 2023, Chapman et al., PRX Q 2023.

*Circuit-level simulation by Rohan Kumar, Sophia Xue, Takahiro Tsunoda

Numerical Simulation

Circuit-level error model for [[4,1,2]]: $\epsilon_1 = 11.5\%, \epsilon_2 = 8.1\%$

Noise hierarchy is important: $(1 - \epsilon_{\text{detectable}} - \epsilon_{\text{undetectable}}) \gg \epsilon_{\text{detectable}} \gg \epsilon_{\text{undetectable}}$

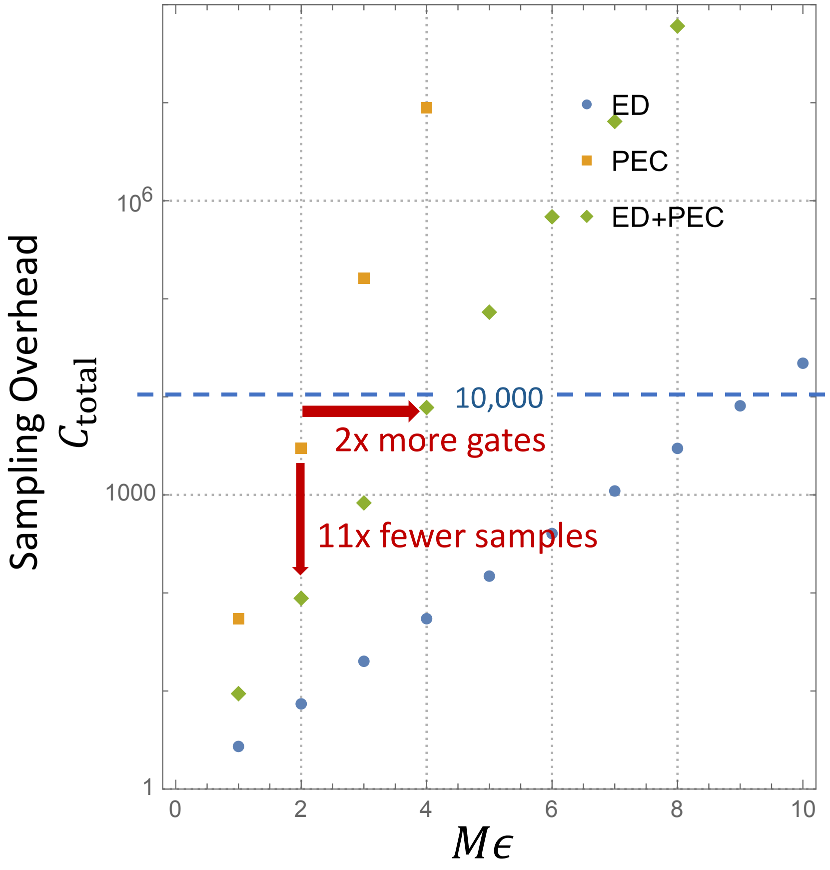
Focusing on circuit size M, where $M\epsilon \approx 1$

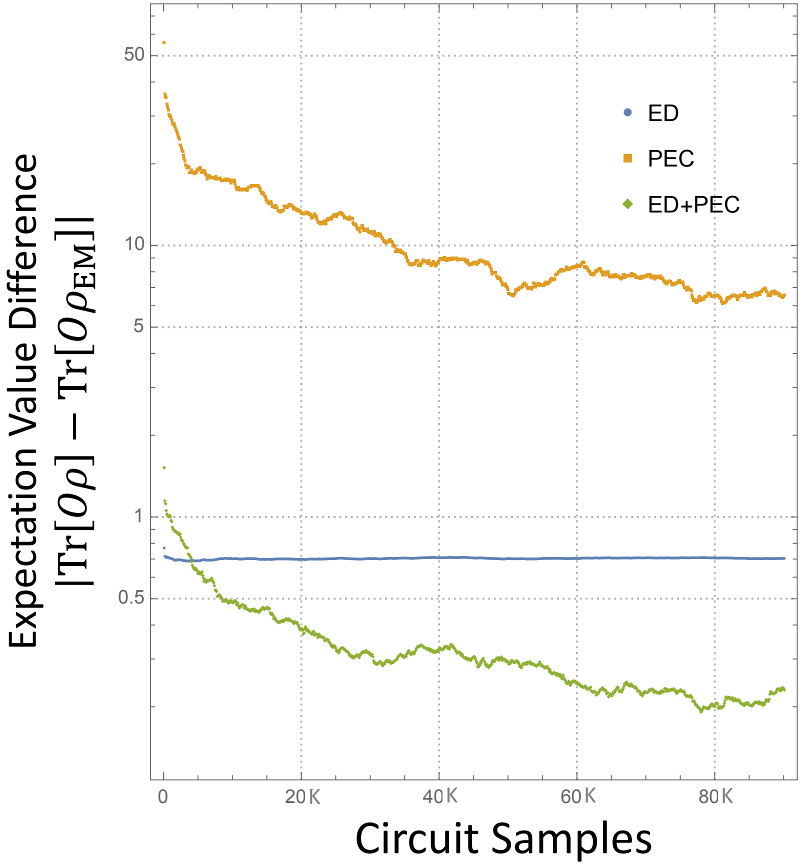
Sampling overhead scaling:

ED alone: $\exp(M\epsilon_1)$

PEC alone: $\exp(4M(\epsilon_1+\epsilon_2))$

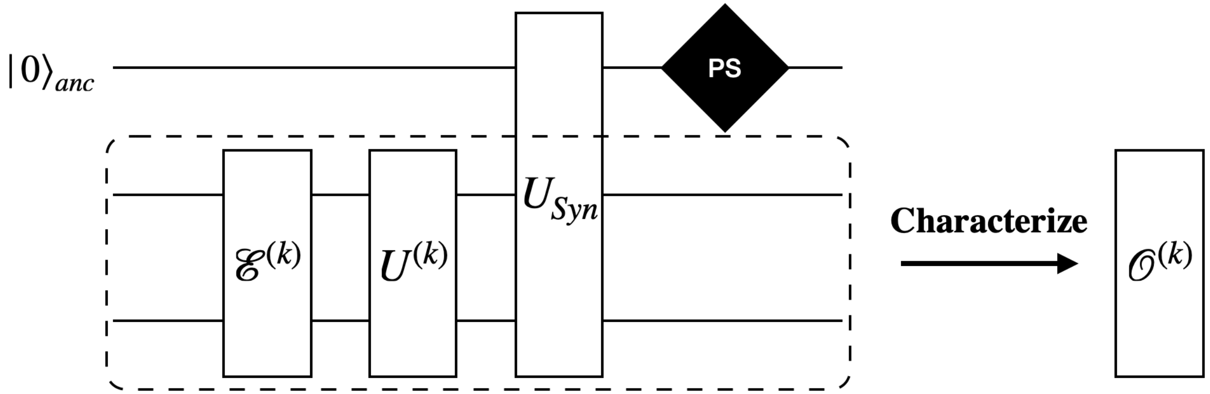
ED+PEC: $\exp(M\epsilon_1 + 4M\epsilon_2)$





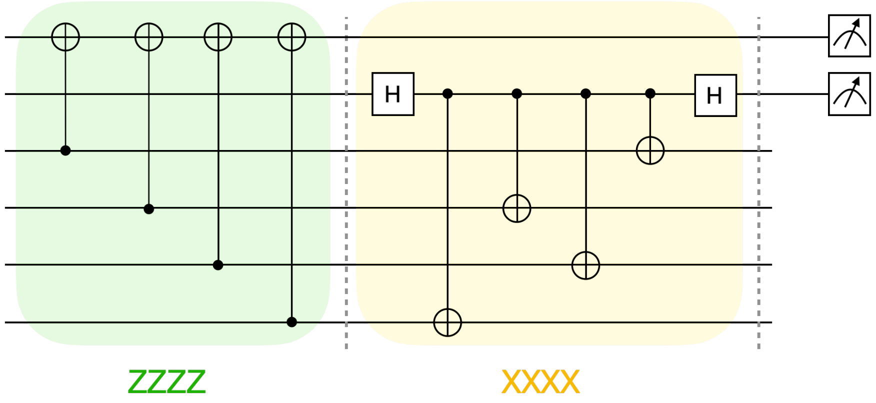
Characterizing Imperfect Error Detection

Characterize post-selected channel of an **error-detected gate**:

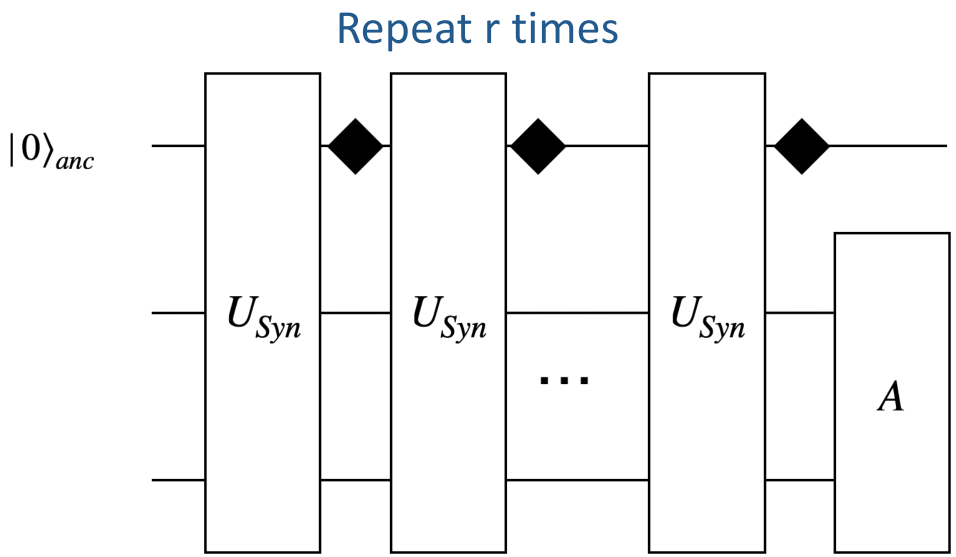


[[4,2,2]] code **logical subspace** basis:

$$|00\rangle_L = (|0000\rangle + |1111\rangle)/\sqrt{2}$$
$$|01\rangle_L = (|0011\rangle + |1100\rangle)/\sqrt{2}$$
$$|10\rangle_L = (|0101\rangle + |1010\rangle)/\sqrt{2}$$
$$|11\rangle_L = (|0110\rangle + |1001\rangle)/\sqrt{2}$$



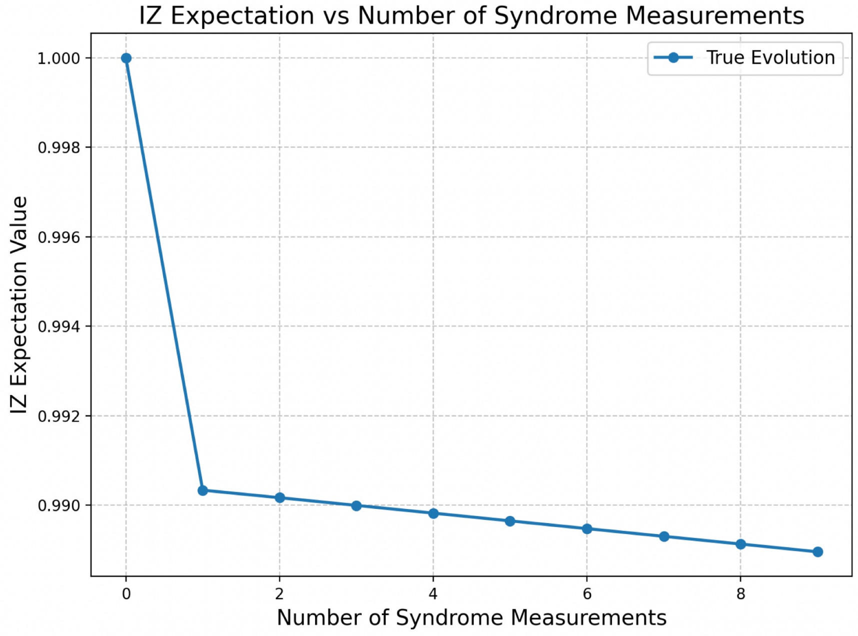
Logical Observable After Repeated Error Detections



Experimental setup:

(assuming a physical Markovian error channel)

1. Start in a (perfect) logical state, say $|00_L\rangle$
2. Apply repeated error detection & post-selection r times
3. Log the expectation of an observable, say $A = I \otimes Z$
4. Plot the Observable Expectation vs Num. Detection Cycles



Simulation details:

- [[4,2,2]] code: 4 data qubits, 2 ancilla qubits
- Hamiltonian-level noise via Lindblad's master equation in QuTiP.
- Including Pauli errors (single-qubit and two-qubit), meas. errors.

Transition Matrix Analysis

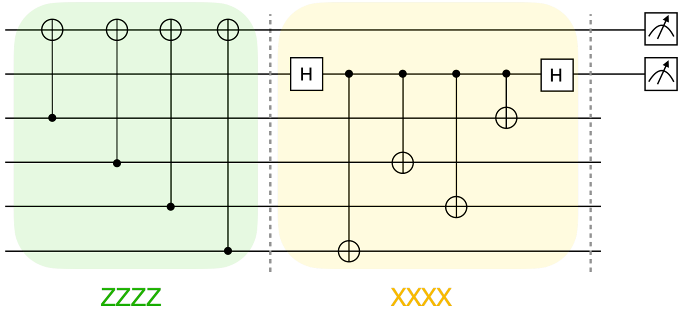
For each syndrome measurement cycle

$$C_i = \begin{cases} \text{Correct logical state} & i = 0 \\ \text{Incorrect logical state} & i = 1 \\ \text{Undetected leakage state} & i = 2 \\ \text{Detected leakage state} & i = 3 \end{cases}$$

Circuit-level Pauli noise model
Errors happen randomly at any point in the circuit

$$\xrightarrow{\textbf{Construct}} \quad 64\left\{ \overbrace{\begin{pmatrix} a_{1,1} & a_{1,2} & \cdots & a_{1,64} \\ a_{2,1} & a_{2,2} & \cdots & a_{2,64} \\ a_{3,1} & a_{3,2} & \cdots & a_{3,64} \\ \vdots & & & \\ a_{64,1} & a_{64,2} & \cdots & a_{64,64} \end{pmatrix}}^{64} \right. \quad \xrightarrow{\textbf{Reduce}} \quad \begin{pmatrix} T_{00} & T_{01} & T_{02} & T_{03} \\ T_{10} & T_{11} & T_{12} & T_{13} \\ T_{20} & T_{21} & T_{22} & T_{23} \\ 0 & 0 & 0 & 1 \end{pmatrix}$$

[[4,2,2]] **syndrome extraction** circuit:



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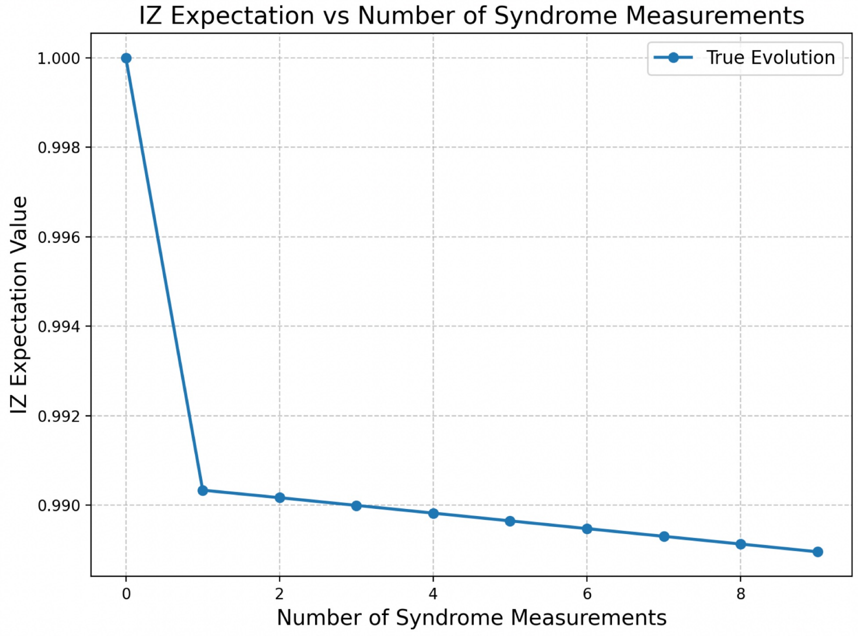
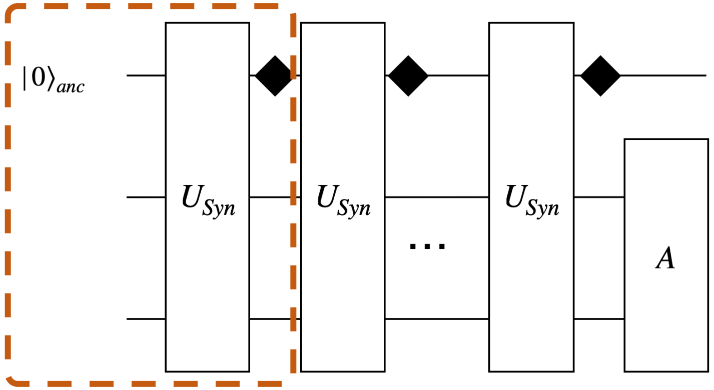


With repeated ED, it reaches **stationary** dynamics: Leakage out v.s. seepage back into the logical subspace.

Characterizing Error Detections

Naïve logical quantum process tomography (QPT):



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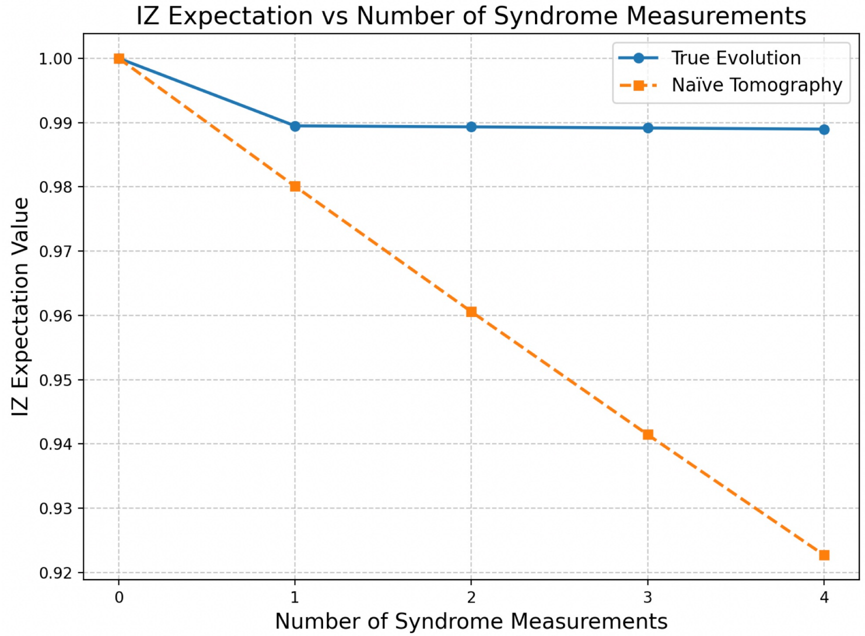

Characterizing Error Detections

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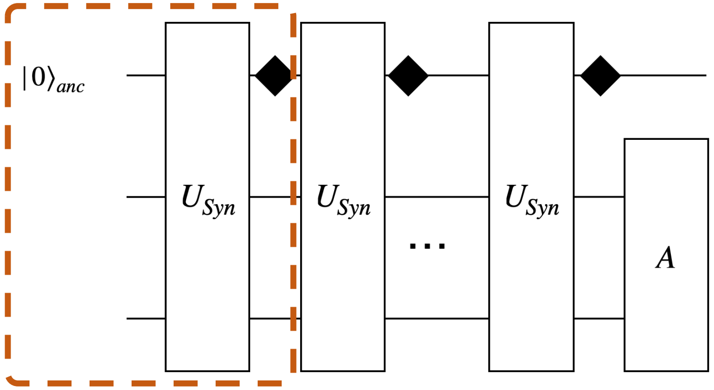
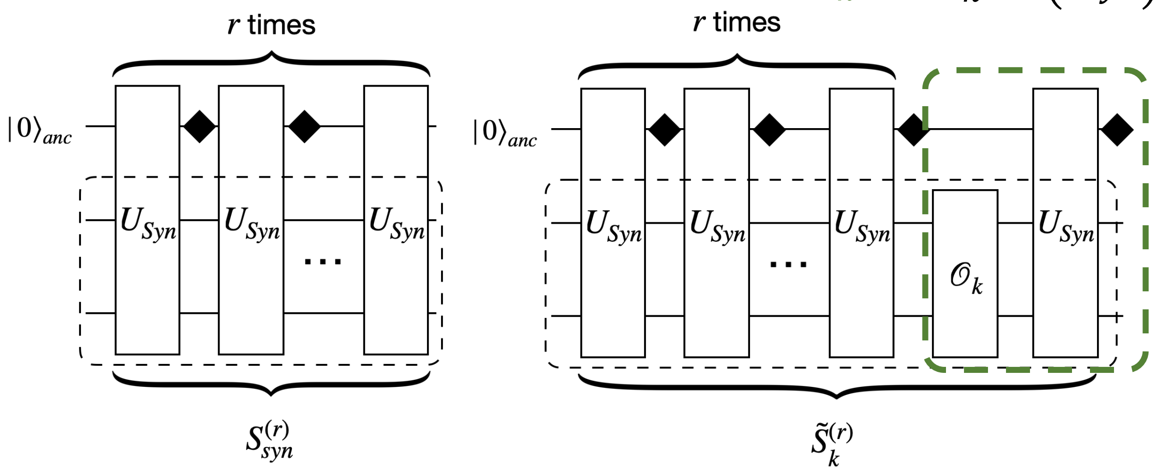


Super-operator inversion technique: $S_k^{(r)} = \widetilde{S_k^{(r)}} \cdot \left(S_{syn}^{(r)}\right)^{-1}$



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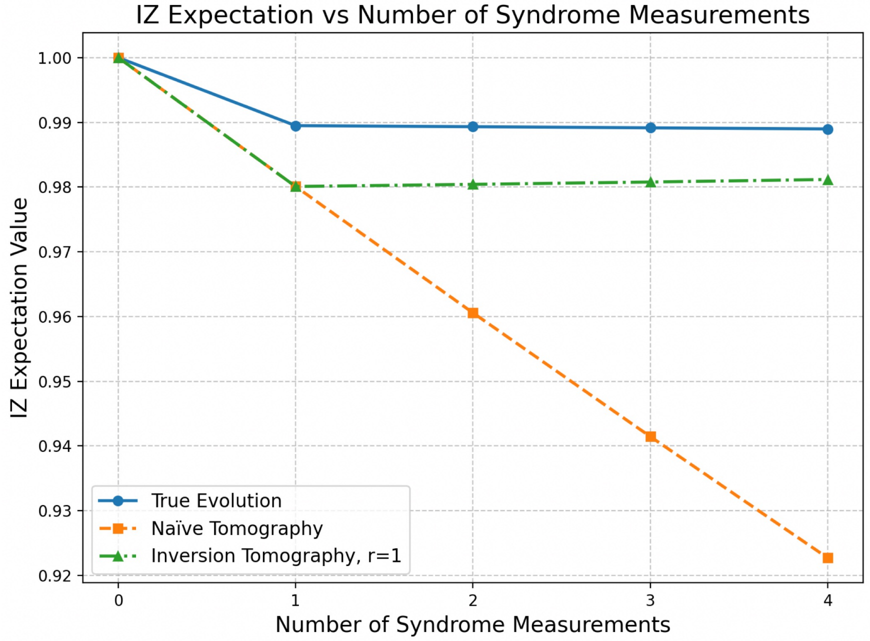
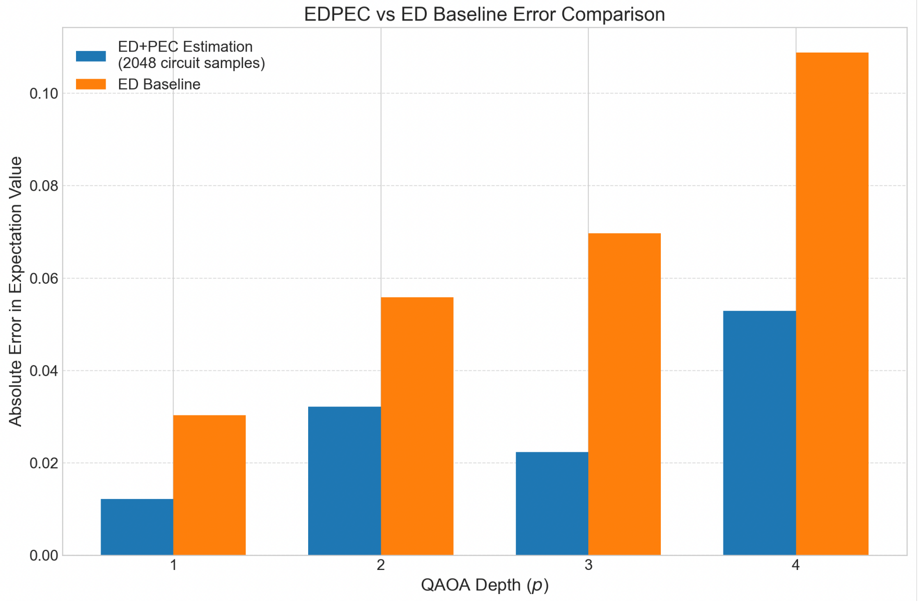


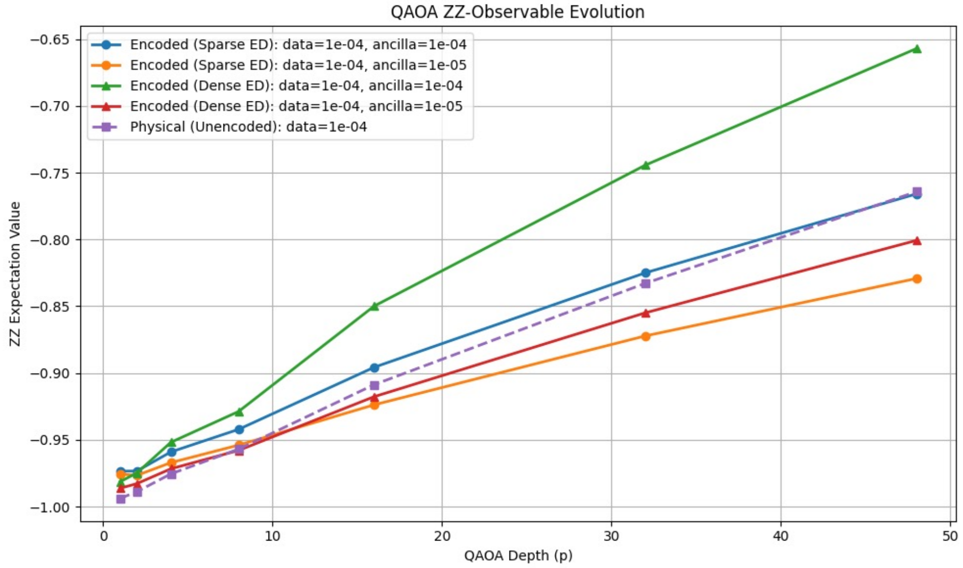
Error Detection + Error Mitigation

PEC can remove the bias coming from **well-characterized** residual undetected error



Cadence of mid-circuit detection is important:

- Error detection itself is noisy (2Q: 10 unit time, ED: 80 unit time)
- To locate error events in space and time and prevent “seepage” back into logical subspace.



More factors to consider in experiments:

- Gate set tomography of error-detected gates
- Ratio of detectable/undetectable errors

R. Kumar, T. Tsunoda, S. Xue, D. Li, R. Schoelkopf, Y. Ding. In preparation (2025).

Error-Corrected Qubits

Even an exact decoder makes mistakes

$$p_L = \prod_{e \in E} p_e \prod_{e \notin E} (1 - p_e), \quad \hat{p}_L = \frac{p_L}{\sum_{L \in \{X,Y,Z,I\}} p_L}$$

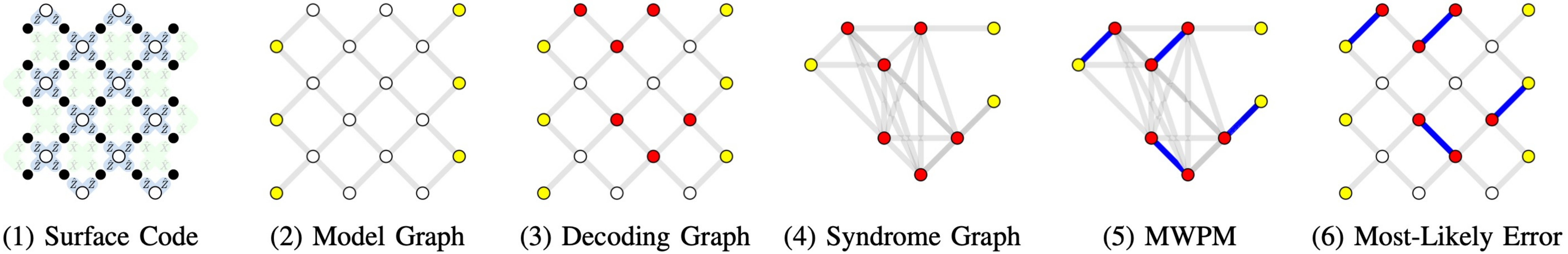


Figure taken from Fusion Blossom (by Wu et. al.) Figure 1, with author's permission.

Syndromes from surface code experiment → Modified decoder: Logical channel estimator → Logical expectation value estimation via quasi-probability simulation

$\mathcal{N}^{-1} = \sum_j \eta_j \widetilde{L_j}$, $\widetilde{L_j}$ =logical Pauli channel

Traditional decoder: Syndromes from surface code experiment → Error likelihood estimator → Most-likely Error

$$\arg \max_{\mathcal{E}|S(\mathcal{E})=\mathcal{S}} \prod_{e \in \mathcal{E}} \frac{P(e)}{1 - P(e)}$$

Estimate the **posterior probability of logical equivalent classes** given syndrome pattern s.

Logical equivalent classes differ by logical Pauli operators

$$p_{\bar{L}} \equiv p(\bar{L}|s) = \frac{p(\bar{L}, s)}{p(s)}, \bar{L} \in \otimes^k P$$

Logical Pauli channel (due to partial information from syndrome)

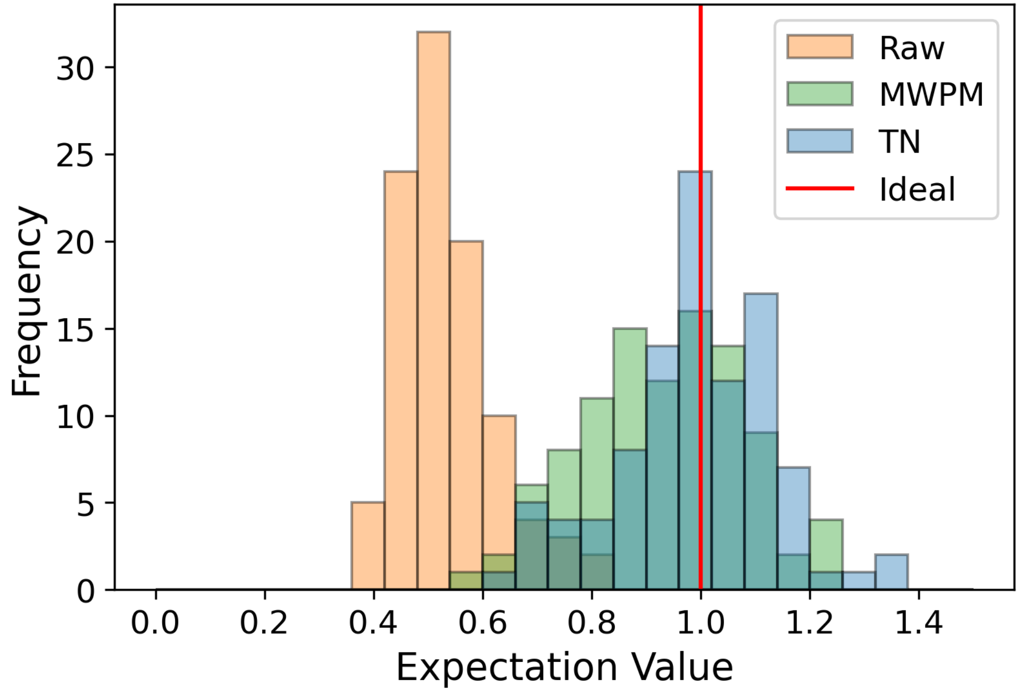
$$\tilde{L}(\rho) = \sum p_{\bar{L}} \bar{L} \rho \bar{L}^\dagger$$

E.g., For a surface code patch: $\bar{L} = I, X, Z, Y$

Characterizing and mitigating decoding errors

Characterization bias of posterior probability $p(\bar{L}|s)$ of logical equivalent classes: (a) $\bar{L} = I$,(b) $\bar{L} = X$, (c) $\bar{L} = Z$, (d) $\bar{L} = Y$

100 **random Clifford circuits** (q=5), each run 1000 shots



Raw: Unmitigated exact decoder
MWPM: Mitigation + MWPM decoder
TN: Mitigation + TN decoder

Z. Zhou, S. Pexton, A. Kubica, Y. Ding. In Preparation (2025)

Outlook: (early) FT devices will operate at the verge of failure

Talk Summary:

Characterizing imperfect error detections:

- Non-Markovian logical dynamics.
- Super-operator inversion technique.

For actual ED gain, noise hierarchy is important:

$$(1-\epsilon_{\text{detectable}}-\epsilon_{\text{undetectable}}) \gg \epsilon_{\text{detectable}} \gg \epsilon_{\text{undetectable}}$$

Mid-circuit detection is also important:

- To locate error events in space and time.
- To prevent “seepage” back into logical subspace.

Characterizing error-corrected logical channels:

- Syndrome information for logical channel estimation

Future Directions:

Logical channel learning:

- ED/EC channels

Experimental demonstration:

- Choice of ED/EC codes + PEC

Evaluation in FTQC:

- Characterizing logical gates
- Transversal, lattice surgery, etc.

Acknowledgement

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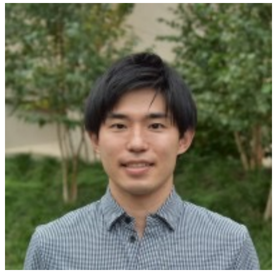

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Thank You!